

# Study on Fabrication Process of 10×10 Array High-Frequency Wireless QCM Chip

Junki Shinohara<sup>1†</sup>, Manabu Yoshino<sup>1</sup>, Manabu Suzuki<sup>1</sup>, Noriyasu Masumoto<sup>1</sup>, Fumihito Kato<sup>1</sup> and Hirotsugu Ogi<sup>2</sup> (<sup>1</sup>Dept. Mech. Eng., Nippon Inst. of Tech.; <sup>2</sup>Grad. Sch. Eng., Osaka Univ.)

## 1. Introduction

The quartz crystal microbalance (QCM) is a device which can sensitively detect substances with very small masses<sup>1)</sup>. The QCM can detect the mass loading due to the adsorption of the target substance on the surface of the quartz resonator, which vibrates at the through-thickness shear-vibration mode, as the resonance frequency change. In addition, it is a mass detection type sensor which can measure the reaction process on the surface of the quartz resonator in real time. Therefore, it is difficult to detect low molecular weight substances. In conventional QCMs, metal electrodes (e.g., Au-Cr) for excitation and signal detection are formed on both sides of the quartz resonator. The quartz is a piezoelectric material and it is excited by applying an electric field through the inverse piezoelectric effect. At the same time, the vibrating quartz resonator generates the electric-polarization charge by the piezoelectric effect, therefore the resonance frequency can be measured by detecting it with the metal electrodes. The sensitivity of the QCM is inversely proportional to the square of the thickness of quartz resonator<sup>2)</sup>, hence the fundamental resonance frequency increases and the sensitivity improves as the quartz thickness decreases. However, because the inertial resistance due to the metal electrodes formed on both sides of the quartz resonator increases as the quartz thickness decreases, the quartz resonator is gradually not to vibrate. In addition, because thin quartz crystal is very fragile, it will be damaged during handling. As a result, most of the quartz resonators used in commercially available QCM have a thickness of 50 to 330  $\mu\text{m}$  (fundamental resonance frequency: 5-33 MHz). Commercially available QCM has the following issues in addition to the sensitivity. Temperature compensation is needed because the temperature characteristics are caused by the difference in the thermal expansion coefficient between the quartz resonator and the metal electrodes. Furthermore, the simultaneous sensing of many samples requires the same number of measurement cells, which makes the apparatus large. In addition, the structural damping occurs because the quartz resonator is mechanically fixed in the measurement cell, and the quality factor (Q-factor) decreases. In this study, to

improve these issues, we propose a 10 by 10 array high-frequency wireless electrodeless QCM chip and investigate the fabrication process using the silicon (Si) anisotropic-etching technique. This study focuses on the process construction for fabricating the diaphragm-shaped resonator array. Accordingly, the Si substrate with the thermal oxide layer ( $\text{SiO}_2$ : 2.5  $\mu\text{m}$ , Si: 525  $\mu\text{m}$ ) was used instead of the Si substrate on which the quartz layer was bonded in this investigation.

## 2. Proposal of 10 by 10 array QCM chip

Figure 1(a) shows an external view of a 10 by 10 array wireless electrodeless QCM chip. The chip size is  $15 \times 15 \times 0.525 \text{ mm}^3$ . Figure 1(b) shows the cross-section of the diaphragm assuming the resonator.

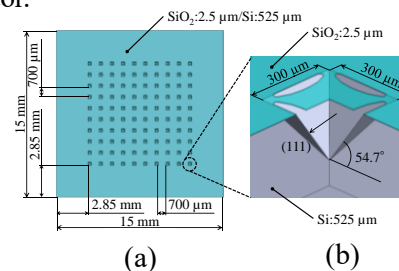


Fig.1 10 by 10 array wireless electrodeless QCM chip: (a) External view and (b) cross-section

In this research, a small chip with a minimum pitch between the diaphragms is fabricated by etching from the upper side of the Si (100) substrate. At that time, by optimizing the shape of etching holes on the upper side of the Si (100) substrate, an inverted pyramid structure with an inclination of 54.7 degrees is formed. The fabrication of the diaphragm with a side length of 0.1 mm to 0.5 mm is investigated. By applying this process, 100 or more diaphragm resonators with a thickness of a few  $\mu\text{m}$  can be fabricated on one chip. Therefore, the added value of wireless QCM can be greatly enhanced, as it is not necessary to connect several measurement cells.

## 3. Fabrication process

Figure 2 shows the fabrication steps of the 10 by 10 array high frequency wireless electrodeless QCM chip. At first, the Si substrate with the

thermal oxide layer ( $\phi 4$  in.,  $\text{SiO}_2$ : 2.5  $\mu\text{m}$ , Si: 525  $\mu\text{m}$ ) was divided into small pieces with a side length of 15 mm by the dicing saw (**Fig. 2(a)**). The small pieces were heat-treated using a hot plate (120  $^\circ\text{C}$ , 5 min) for dehydration, and then the negative resist (OMR-100, Tokyo Ohka Kogyo) of about 2  $\mu\text{m}$  was spin-coated on the surface of the small pieces considering the process simplification and corrosion resistance (**Fig. 2(b)**). After prebaking the small pieces, ultraviolet ray was applied to them for 2 s using the contact mask aligner (LA410nk, Nanotec) (**Fig. 2(c)**). Subsequently, the small pieces were rinsed by alternately immersing them in the resist developer (OMR developer, Tokyo Ohka Kogyo) and the butyl acetate. After removing the solvent by rinsing with distilled (DI) water, they were post-baked (150  $^\circ\text{C}$ , 5 min) using the hot plate (**Fig. 2(d)**). And then, the small pieces were immersed in the buffered hydrofluoric acid solution ( $\text{NH}_4\text{F}(40\%):\text{HF}(50\%)=5:1$ ), and the  $\text{SiO}_2$  layer was removed by the wet etching (25 min) using the negative resist as the mask. They were rinsed with DI water after the wet etching (**Fig. 2(e)**). After that, the small pieces were immersed in the piranha solution ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2(30\%)=3:1$ ) to remove the negative resist and the organic materials, and they were rinsed with DI water. Subsequently, the small pieces were immersed in the tetramethylammonium hydroxide (TMAH) solution (25%), and Si anisotropic etching was then performed for about 4 hours heating at 75  $^\circ\text{C}$  using the heater (**Fig. 2(f)**). After observing that the wet etching stopped with the Si (111) surface exposed, the small pieces were rinsed by immersing them in DI water so that no TMAH residue remained (**Fig. 2(g)**).

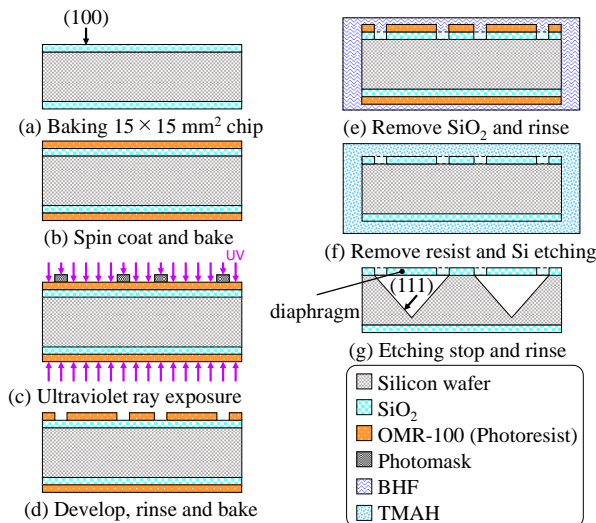


Fig. 2 Fabrication steps of 10 by 10 array wireless electrodeless QCM chip.

#### 4. Result and Discussion

The fabrication process of the diaphragm with a side length of 0.1 mm to 0.5 mm was investigated.

Because the negative resist was used in this study, the fine patterns were obtained only the resist mask for which they form the diaphragm with a side length of 0.3 mm to 0.5 mm. Therefore, when the  $\text{SiO}_2$  layer was wet-etched, it could be completely removed with a mask for forming the diaphragm with a side length of 0.3 mm to 0.5 mm. However, when using a resist mask with a side length of 0.1 mm to 0.2 mm, the fresh etching solution was not circulated to the details of the pattern, and the  $\text{SiO}_2$  layer was not sufficiently removed. Based on these results, Si anisotropic etching using TMAH was performed for the diaphragm with a side length of 0.3 mm to 0.5 mm. As a result, we succeeded in fabricating the diaphragm with a side length of 0.3 mm with a yield of 85% or more. **Figure 3(a)** is a photographic image in which the pitches between the diaphragms of the fabricated 10 by 10 array QCM chip are omitted. Because Si thermal oxide layer has an internal compressive stress of several hundred MPa, the diaphragms warp due to the buckling. **Figure 3(b)** shows a cross-section of Si thermal oxide layer observed using a scanning electron microscope (SEM). Because the thickness is about 2.4  $\mu\text{m}$ , the fundamental resonance frequency corresponds to about 700 MHz when the diaphragm resonator is fabricated using a thin quartz.

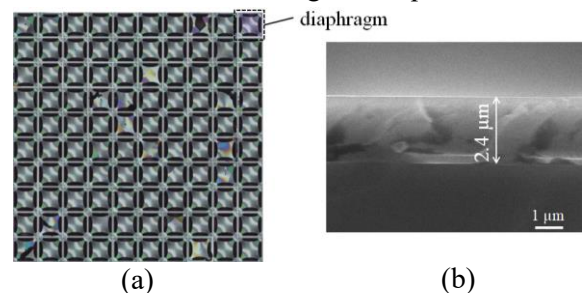


Fig. 3 (a) Photographic image of array chip and (b) cross-section of diaphragm

#### 5. Conclusion

We proposed a 10 by 10 array high-frequency wireless electrodeless QCM chip. Through the trial production of the device, a simple fabrication process using a negative resist was constructed. We succeeded in fabricating a 10 by 10 array QCM chip which has the diaphragms with a side length of 0.3 mm and a thickness of about 2.4  $\mu\text{m}$ . In this study, because Si thermal oxide layer was used as the diaphragm, buckling occurred due to internal stress. However, a yield of 85% or more per chip was achieved.

#### References

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